REMARKS

In response to the above-identified Office Action, Applicants have amended the application and respectfully request reconsideration thereof. Applicants respectfully submit that the amendments to the pending claims are not done to overcome the rejections of these claims by the Examiner but rather to expedite the prosecution of the present application and to emphasize and concisely claim the various features of the present invention.

Claims Rejections under 35 U.S.C. §103

Claims 9-20 and 22-34 have been rejected under 35 U.S.C. §103(a) as being anticipated by U.S. Patent No. 4,779,276 to Kashida et al. (hereinafter referred to as Kashida) in view of U.S. Patent No. 6,445,702 to Wright (hereinafter referred to as Wright).

Claim 21 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Kashida and Wright in view of U.S. Patent No. 5,905,741 to Matsukuma et al. (hereinafter referred to as Matsukuma).

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in Applicants' disclosure." In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicants respectfully submit that claims 9-34, as amended, are not rendered obvious by Kashida, Wright, and/or Matsukuma, for the reasons and explanations set out below.

With respect to the amended claim 9, Applicants respectfully submit that Kashida and Wright do not teach, disclose, or suggest all the limitations of claim 9. In particular, they do not teach or suggest the following elements of claim 9:

> "receiving a plurality of information bits, the plurality of information bits *containing different classes of information bits*;

> determining an outer quality metric in accordance with the plurality of information bits and *an inner quality metric in accordance with at least one group of information bits of a particular class*; and
> forming a frame comprising the plurality of information bits, the outer quality metric, and the inner quality metric, the outer quality metric being used for protection of the plurality of information bits and the *inner quality metric being used for protection of the at least one group of information bits of the particular class*." (emphasis added)

As explained in Applicants' response to the previous Office Action, Kashida discloses a data transmission system including components for generating error detecting-correcting data and for dispersing the error detecting-correcting data in the information data (Kashida, Abstract, Col. 2, lines 49-63). More specifically, Kashida discloses a recording system of a digital VTR in which incoming digital data is supplied to a mapping coding circuit to generate mapping coded digital data that is temporarily stored at a memory (Kashida, Col. 10, lines 20-27, Figure 11). Kashida further discloses that, at the memory, the data is written in a state of excluding the synchronizing data part thereof. An outer code encoding circuit then operates to add outer code check digits as follows. In the case of conventional arrangement shown in Figure 2 of Kashida, a computing operation is performed on the vertical column of the information data and the check digits are added to the same column. In the other case, the encoding starting point of one column is arranged to differ from another column as to have the outer code digits allocation as shown in Figure 9 of Kashida. According to Kashida, after the data is arranged to have the outer code check digits allocated as shown in Figure 9, the data is read out sidewise. Then, an inner code encoding circuit adds an inner code digit point to each of the rows of data that are read out sidewise (Kashida, Col. 10, lines 42-67, Figures 9-11).

However, Kashida fails to disclose or suggest any mechanism or method to form a frame which includes *different classes of information bits*, an outer quality metric for protection of information bits in the frame and an inner quality metric for protection of a *portion or group of information bits of a particular class*. More specifically, Kashida does not disclose or suggest that the outer code check digit is for protection of a frame and the inner code check digit is for protection of a portion of the respective frame which contains information bits of a particular class. On the contrary, as illustrated by Figures 2 and 9 of Kashida and the description thereof,

the arrangement of data as disclosed in Kashida is a two-dimensional arrangement of multiple frames where each row corresponds to a data frame. In particular, it is stated by Kashida that "FIG. 2 shows a case wherein *a plurality of data frames* each of which is arranged as shown in FIG. 1 and is provided with *an inner code (row check code)* are *vertically aligned with an outer code (column check code)* arranged in a vertical direction" and that the arrangement forms a product code (Kashida, Col. 2, lines 17-25, Figures 1-2). Furthermore, Kashida states that, in reference to Figures 9 and 10, after completion of transfer of all data from the synchronizing data to the *inner code check digit within one data frame, a data frame of a next row* is transferred. Therefore, it is clear that the inner check code as described in Kashida is for a frame (a row) in the two-dimensional arrangement of multiple frames. The inner check code as described in Kashida does not correspond to *a group of information bits of a particular class in a frame which contains different classes of information bits.*

Again, Applicants cannot find any disclosure or suggestion by Kashida that is directed to a frame containing information bits of different classes in which an outer quality metric is used for the protection of the frame and in which an inner quality metric is used for the protection of a portion of the frame which contains information bits of a particular class. Therefore, Applicants respectfully submit that Kashida does not teach, suggest, or provide any motivation for a method as claimed in the amended claim 9 of the present application.

As explained in the response to the previous Office Action, Wright discloses a method for organizing a plurality of cells into a fixed size frame comprising the steps of: (a) determining an inner coding rate for a first set of data cells; (b) forming a group of codewords by applying an outer code to the first set of data cells; (c) entering the group of codewords row wise into an interleaving array; and (d) applying an inner code column wise to the group of codewords, thereby forming a fixed size frame body (Wright, Abstract, Col. 1, lines 35-45, Figures 2 and 4).

However, Applicants respectfully submit that Wright does not teach, disclose or suggest the above-recited elements of the amended claim 9. Specifically, Wright discloses that the method for organizing the plurality of data cells into a fixed size frame for transmission is performed as follows. First, an inner coding rate is determined for the next frame to be formed. A group of codewords are then formed by applying the outer code to a set of data cells such that the number of codewords formed is based on the inner coding rate. A rectangular array is used

for interleaving between the codes. To format the array, the group of codewords are placed row wise into the interleaving array, partially filling it. Next, the contents of the array are expanded by applying the inner code to the columns of this array. (Wright, Col. 3, lines 1-22, Figure 2 and 4). Thus, it can be seen that the method that is disclosed by Wright is very different and highly distinguishable from the method as claimed in claim 9.

In addition, the frame structure and format (the results) generated by the method disclosed in Wright is very different than the frame structure generated by the method of the present invention as claimed in the amended claim 9. Specifically, Applicants are unable to find any disclosure or suggestion by Wright regarding a frame that contains different classes of information bits, an outer quality metric, and at least one inner quality metric for protection of a group of information bits which corresponds to a particular class, as claimed in the claim 9.

Because Kashida and Wright do not teach or suggest all the limitations of the amended claim 9, Applicants respectfully submit that claim 9, as amended, is not rendered obvious by Kashida and Wright, either alone or in combination. Since claims 10-15 depends from claim 9 and includes additional elements/features, these claims are also not anticipated or rendered obvious by Kashida and/or Wright. Accordingly, Applicants respectfully request that the rejection of claims 9-15 be withdrawn.

Similarly, Applicants respectfully submit that claims 16-34 are also not rendered obvious by Kashida and Wright, for the reasons and explanations provided above with respect to the amended claim 9.

As explained above, Kashida and Wright do not disclose, suggest or provide any motivations regarding a frame having the frame structure and content as claimed in claims 16-34. Specifically, they do not teach or suggest any frame structure containing a plurality of information bits of different classes, an outer quality metric for the protection of the plurality of information bits, and an inner quality metric for the protection of one group of information bits that corresponds to a particular class.

Furthermore, Kashida and Wright do not disclose or suggest any method or mechanism for *partial recovery of a frame* as claimed in claims 16-34. Specifically, Applicants are unable to find any disclosure or suggestion by Kashida and Wright for recovering *a portion of a frame containing information bits of a particular class* using an inner quality metric which corresponds

to that portion of the frame when the entire frame has not been correctly received as indicated by the outer quality metric.

With respect to claim 21, it is stated in the Office Action that Kashida and Wright substantially teaches the claimed invention as described in claim 20 from which claim 21 depends and that Matsukuma teaches that frames are discarded. As explained above, Kashida and Wright do not disclose, suggest or provide any motivations regarding a frame having the frame structure and content as claimed in claim 20. Specifically, Applicants are unable to find any disclosure or suggestion by Wright regarding a frame that contains an outer quality metric for protection of the frame and at least one inner quality metric for protection of a portion of the frame which contains information bits of a particular class. Similarly, there is no disclosure or suggestion in Matsukuma regarding the specific limitations claimed in claim 20. Furthermore, Kashida, Wright, and Matsukuma do not disclose or suggest any method or mechanism for *partial recovery of a frame* as claimed in claim 20. Specifically, Applicants are unable to find any disclosure or suggestion by Kashida, Wright, and Matsukuma for recovering *a portion of a frame containing information bits of a particular class* using an inner quality metric corresponds to that portion of the frame when the frame has not been correctly received as indicated by the outer quality metric.

Accordingly, Applicants respectfully request that the rejection of claims 16-34 be withdrawn.

REQUEST FOR ALLOWANCE

In view of the foregoing, Applicants submit that all pending claims in the application are patentable. Accordingly, reconsideration and allowance of this application are earnestly solicited. Should any issues remain unresolved, the Examiner is encouraged to telephone the undersigned at the number provided below.

Respectfully submitted,

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